Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Sixth Semester

Electrical and Electronics Engineering

EE3011 - Multilevel Power Converters

Regulations - 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	List the different topologies of multilevel converter?	UN	1	2
2.	Explain about asymmetric topology.	UN	1	2
3.	Compare Unipolar and bipolar PWM topologies.	UN	2	2
4.	What is phase-shifted multicarrier modulation?	RE	2	2
5.	Show the converter structure of diode clamped converter.	RE	3	2
6.	Explain the advantages of diode clamped converter.	UN	3	2
7.	What are the modes of operation in flying capacitor multilevel inverter?	RE	4	2
8.	Recall the circuit diagram for flying capacitor multilevel inverter.	RE	4	2
9.	How can you reduce the number of switches in a converter?	RE	5	2
10.	Classify the different pulse generation methods.	UN	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	Build a converter topology for common dc bus .	AP	1	13
		Or			
	b	Organize the functions of converter derived from symmetric topology without a DC link.	AP	1	13
12.	a	Construct various types of modulation techniques used in H bridge inverter.	AP	2	13
		Or			
	b	Develop in detail about the working of phase shifted and level shifted PWM techniques used in a H bridge inverter.	AP	2	13
13.	a	Model the structure of a diode clamped multilevel inverter.	AP	3	13
		Or			

	b	Examine the effectiveness of voltage balancing in DCMC converter.	AN	3	13
14.	a	Explain in detail about the modulation scheme in flying capacitor multilevel converter.	UN	4	13
		Or			
	b	How dynamic voltage balancing is done in flying capacitor multilevel converter.	UN	4	13
15.	a	Develop a multilevel converter with reduced switch count.	AP	5	13
		Or			
	b	Analyze the various pulse generation techniques for multilevel converter.	AN	5	13

*PART – C (Marks 1*15 = 15)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
16.	a	Evaluate the pros and cons for symmetric and asymmetric multilevel converter topologies.	EV	1	15
		Or			
	b	Build an H bridge inverter and show how it differs from working of a normal inverter and discuss its merits.	EV	5	15